Remarks

Applicant respectfully requests that this Amendment After Final Action be admitted under 37 C.F.R. § 1.116.

Applicant submits that this Amendment presents claims in better form for consideration on appeal. Furthermore, applicant believes that consideration of this Amendment could lead to favorable action that would remove one or more issues for appeal.

Claim 19 has been amended. No claims have been canceled. Therefore, claims 19-35 are now presented for examination.

Claims 19, 21, 25-26, 28, 30 and 35 stand rejected under 35 U.S.C. 103 (a) as being unpatentable over Cheng (U.S. Patent No. 5,694,581) and Jones et al. (U.S. Patent No. 5,619,723) and further in view of Thompson et al. (U.S. Patent No. 6,341,342). Applicant submits that the present claims are patentable over any combination of Cheng, Jones and Thompson.

Cheng discloses a disk array interface system 100 that is compatible and connected to a local bus 105. See Cheng at col. 5, ll. 30-35. The disk array interface system 100 is disclosed an IDE disk array interface system, which includes a bus master to IDE interface chip 110. The bus master to IDE interface chip 110 is connected to two concurrent IDE channels, wherein each includes four dependent IDE subchannels, and each dependent subchannel is connected to two disks. The disk array interface system 100 thus enables data storage and retrieval from sixteen disks via two independent concurrent IDE channels 120 and 130. The bus master to IDE interface chip 110 enables the data transfer to be performed concurrently on IDE channels (col. 5, ll. 42-64). The disk array interface system 100 also includes an array basic input/output system (BIOS) 140 connected, via a data bus and an address bus, to an industrial standard adaptor (ISA) bus 135 which is connected to a main processor, e.g., a motherboard to provide disk array control signals (col. 6, ll. 4-10).

Nevertheless, applicant submits that Cheng does not disclose or suggest an IDE interface coupled to a system bus that receives disk drive requests from a BIOS via the system bus. Cheng discloses an interface coupled to a local bus 105. In addition, Cheng discloses that the interface comprises a BIOS and a data/address bus. Applicant submits that the data/address bus within the interface is not a system bus.

Moreover, since the BIOS and data/address bus referred to by the Office Action is within the interface itself, the transfer of data from the BIOS over the data/address bus it is not analogous to receiving disk drive requests at an interface from an external BIOS via a system bus. Further applicant submits that the local bus 105 disclosed in Cheng is most analogous to a system bus, and that there is no disclosure or suggestion in Cheng of receiving disk drive requests from a BIOS via the local bus 105.

Jones discloses a disk drive array controller. The controller includes a microcontroller CPU with embedded ROM and RAM, a bus interface, and five connected disk drives. The ROM 104 contains the firmware for controller. A system bus coupled to the bus interface provides a communication link between the controller and a host computer, which uses the array of disk drives as secondary memory. See Jones at col. 14, ll. 18-27. However, Jones does not disclose or suggest an IDE interface coupled to a system bus that receives disk drive requests from a BIOS via the system bus.

Thompson discloses an array controller that cleans buffer memory as a background task. The controller includes a transfer buffer, a memory that stores an index or table indicating free and non-zero data sectors within the transfer buffer, and processing logic that uses the transfer buffer for data transfer operations, and when otherwise idle, that scans the index table for contiguous sections of free and non-zero data sectors of the transfer buffer and that zeroes at least one of the contiguous sections. See Thompson at Abstract. Nonetheless, Thompson does not disclose or suggest an IDE interface coupled to a system bus that receives disk drive requests from a BIOS via the system bus.

Claim 19 recites:

> A system comprising:
> a Basic Input/Output System (BIOS);
> a system bus coupled to said BIOS;
> an integrated drive electronics (IDE) interface coupled to said system bus that receives disk drive requests from said BIOS via said system bus;
> a striping controller coupled to said IDE interface;
> a first disk drive including first IDE electronics, said striping controller coupled to said first IDE electronics;
> a second disk drive including second IDE electronics, said striping controller coupled to said second IDE electronics, said first and said second IDE electronics each having data separator electronics, data formatting electronics and head positioning electronics; and
> said striping controller causes data being transmitted between said interface and said first and second drives to be written to and read from the first and second drives in an interleaved form and substantially in parallel.

As discussed above, neither Cheng, Jones nor Thompson disclose or suggest an IDE interface coupled to a system bus that receives disk drive requests from a BIOS via the system bus. Since Cheng, Jones and Thompson fail to disclose or suggest an IDE interface coupled to a system bus that receives disk drive requests from a BIOS via the system bus, any combination of Cheng, Jones and Thompson would also fail to disclose such a limitation.

It is also submitted that Cheng does not teach or suggest a combination with Jones and Thompson, and Thompson and Jones do not teach or suggest a combination with Cheng. It would be impermissible hindsight based on applicant's own disclosure to incorporate the disk interface system in Cheng into the array controllers disclosed in Jones and Thompson, due to different designs. Moreover, such a combination would still lack an IDE interface coupled to a system bus that receives disk drive requests from a BIOS via the system bus.

Therefore, claim 19 is patentable over Cheng and Jones in view of Thompson. Claims 20-24 depend from claim 19 and include additional limitations. As a result, claims 20-24 are also patentable over the combination of Cheng, Jones and Thompson.

Claim 25 recites:

> A method comprising:
> transmitting an integrated drive electronics (IDE) request from a Basic Input/ Output System (BIOS) onto a system bus;
> receiving said IDE request at an IDE interface connected to said system bus;
> transmitting said IDE request to a striping controller coupled to said IDE interface and first IDE electronics of a first disk drive and second IDE electronics of a second disk drive;
> writing to and reading from the first disk drive and the second disk drive in an interleaved form and substantially in parallel in response to said IDE request.

Therefore, for the reasons stated above with respect to claim 19, claim 25 is also patentable over the combination of Cheng, Jones and Thompson. Since claims 26 and 27 depend from claim 25 and include additional limitations, claims 26 and 27 are also patentable over the combination of Cheng, Jones and Thompson.

Claim 28 recites:

> A striping disk controller comprising:
> an integrated drive electronics (IDE) interface coupled to a system bus that receives disk drive requests from a Basic Input/ Output System (BIOS) separately coupled to said system bus; and
> control logic coupled to the IDE interface and first disk electronics of a first disk drive and second disk electronics of a second disk drive, the control logic to cause data being transmitted via the system bus to be written to and read from a first disk drive and a second disk drive in an interleaved form and substantially in parallel.

Thus, for the reasons stated above with respect to claim 19, claim 35 is also patentable over the combination of Cheng, Jones and Thompson. Since claims 36 and 37

depend from claim 35 and include additional limitations, claims 36 and 37 are also patentable over the combination of Cheng, Jones and Thompson.

Claims 20, 22, 27, 29, 31, 34 and 36 stand rejected under 35 U.S.C. 103 (a) as being unpatentable over Cheng (U.S. Patent No. 5,694,581) and Jones et al. (U.S. Patent No. 5,619,723) and Thompson et al. (U.S. Patent No. 6,341,342) in further view of Anderson (U.S. Patent No. 5,905,910). Applicant submits that the present claims are patentable over any combination of Cheng, Jones, Thompson and Anderson.

Anderson discloses a system for the simultaneous operation of multiple disk drives in a computer. The system includes a first disk drive having an interrupt generating circuit to generate a first interrupt signal. The first disk drive receives a first disk transfer command from the computer, processes the first disk transfer command, and generates the first interrupt signal upon completion of the first disk data transfer command. The system also includes a second disk drive, also having an interrupt generating circuit to generate a second interrupt signal. The second disk drive receives a second disk transfer command from the computer while the first disk drive is processing the first disk transfer command such that both the first and second disk drives are simultaneously active. The second disk drive processes the second disk transfer command and generates the second interrupt signal upon completion of the second disk data transfer command. See Anderson at col. 1 ll. 49-65.

However, Anderson does not disclose or suggest an IDE interface coupled to a system bus that receives disk drive requests from a BIOS via the system bus. As described above, neither Cheng, Jones, nor Thompson disclose or suggest a bus interface that communicates directly with BIOS. Therefore, any combination of Cheng, Jones, Thompson and Anderson would also not disclose or suggest such a limitation.

Claims 23, 24, 32 and 33 stand rejected under 35 U.S.C. 103 (a) as being unpatentable over Cheng (U.S. Patent No. 5,694,581) and Jones et al. (U.S. Patent No. 5,619,723) and further in view of Jenkins et al. (U.S. Patent No. 4,047,157). Applicant

submits that the present claims are patentable over any combination of Cheng, Jones, Thompson and Jenkins.

Jenkins discloses a controller for use in a data processing system. Nonetheless, Jenkins does not disclose or suggest an IDE interface coupled to a system bus that receives disk drive requests from a BIOS via the system bus. As described above, neither Cheng, Jones, nor Thompson disclose or suggest a bus interface that communicates directly with BIOS. Accordingly, any combination of Cheng, Jones, Thompson and Jenkins would not disclose or suggest an IDE interface coupled to a system bus that receives disk drive requests from a BIOS via the system bus. Therefore, the present claims are patentable over the combination of Cheng, Jones, Thompson and Jenkins.

Claim 37 stands rejected under 35 U.S.C. 103 (a) as being unpatentable over Cheng (U.S. Patent No. 5,694,581) and Jones et al. (U.S. Patent No. 5,619,723) and Thompson et al. (U.S. Patent No. 6,341,342) in further view of further in view of Mizuno et al. (U.S. Patent No. 5,608,891). Applicant submits that the present claims are patentable over any combination of Cheng, Jones, Thompson and Mizuno.

Mizuno discloses an array type recording system that divides a single circuit into a write circuit and a read circuit. See Mizuno at col. 4, ll. 30-35. However, Mizuno does not disclose or suggest an IDE interface coupled to a system bus that receives disk drive requests from a BIOS via the system bus. As described above, neither Cheng, Jones, nor Thompson disclose or suggest a bus interface that communicates directly with BIOS. Accordingly, any combination of Cheng, Jones, Thompson and Mizuno would not disclose or suggest an IDE interface coupled to a system bus that receives disk drive requests from a BIOS via the system bus. Therefore, the present claims are patentable over the combination of Cheng, Jones, Thompson and Mizuno.

Applicant respectfully submits that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: Aug 21, 2003

Mark L. Watson
Reg. No. 46,322

12400 Wilshire Boulevard
7th Floor
Los Angeles, California 90025-1026
(303) 740-1980